

MATLAB EXPO 2019

Top Down Modeling and Analysis of Analog Mixed-Signal Systems

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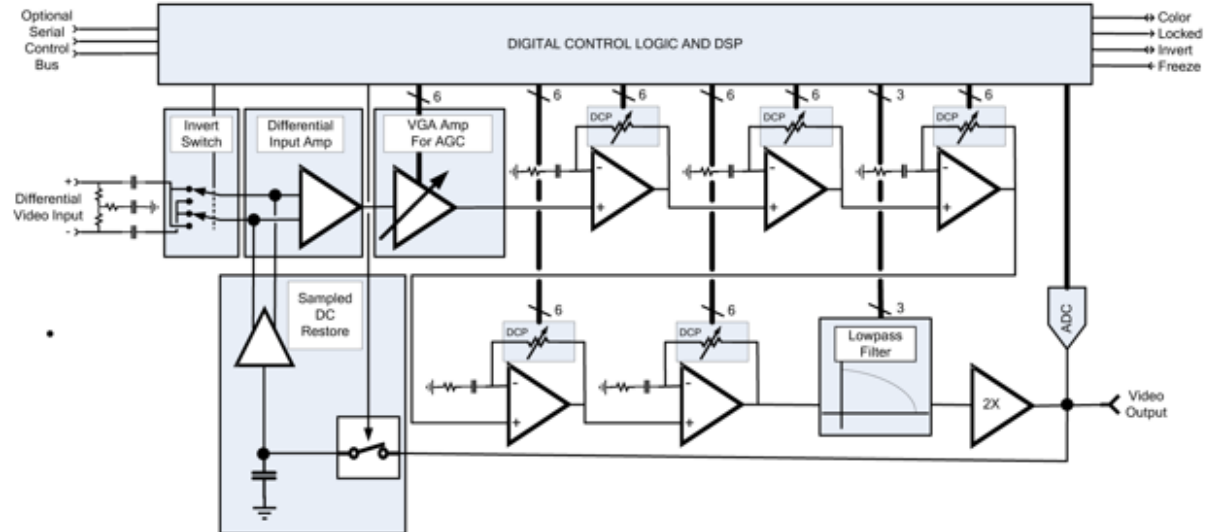
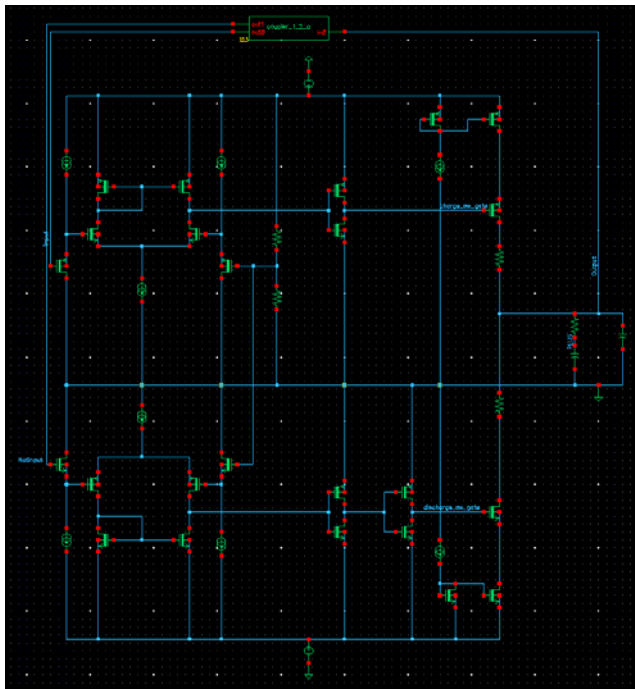


Agenda

- What is Top Down Modeling and Analysis
- Why is Top Down relevant to Analog Mixed-Signal (referred to as AMS)
- Tools, Flows and Methodology to support a Top Down AMS workflow
- Using a Top Down AMS Workflow to implement
 - Phased Locked Loop
 - Analog to Digital Converter
 - SerDes (was covered in previous talk)

What is Bottoms-up Analysis

Assemble AMS building blocks and analyze via simulation
 AMS building blocks: MOS, BJT, Diodes, Resistors, Capacitor, Logic Gates



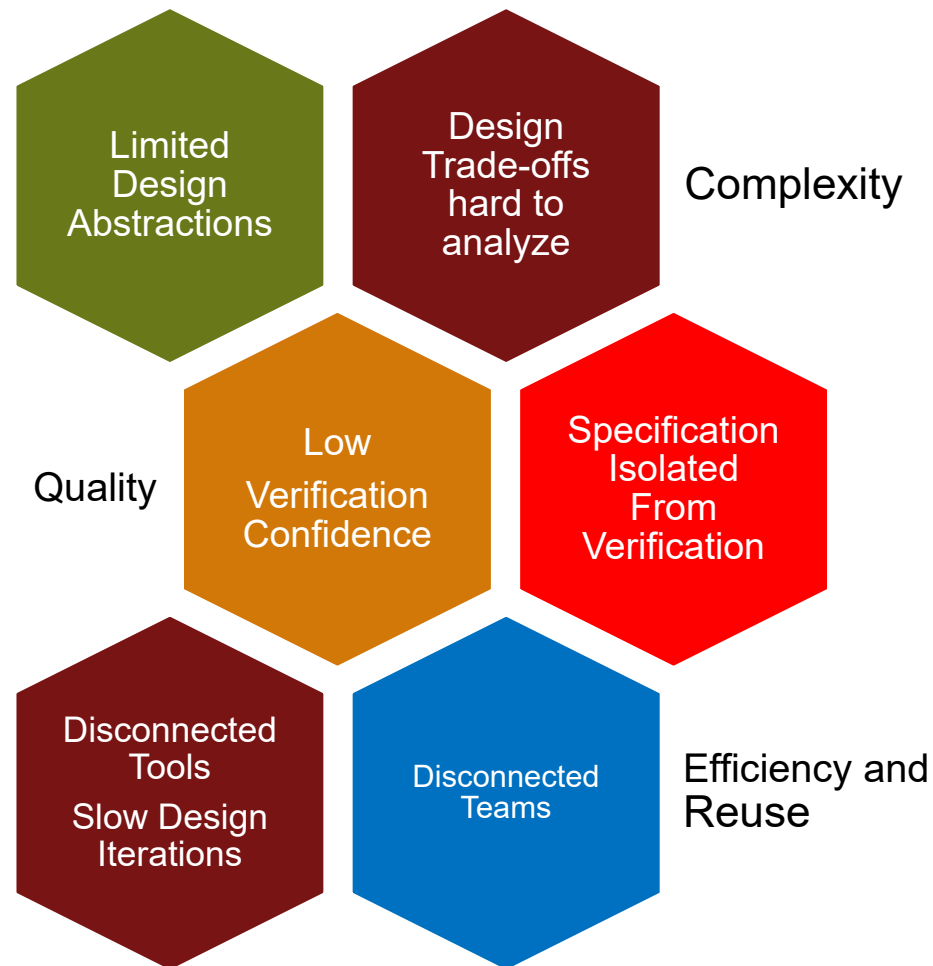
MATLAB EXPO 2019 Charge Pump

Simulation Time: Seconds to Minutes

Video Cable Equalizer

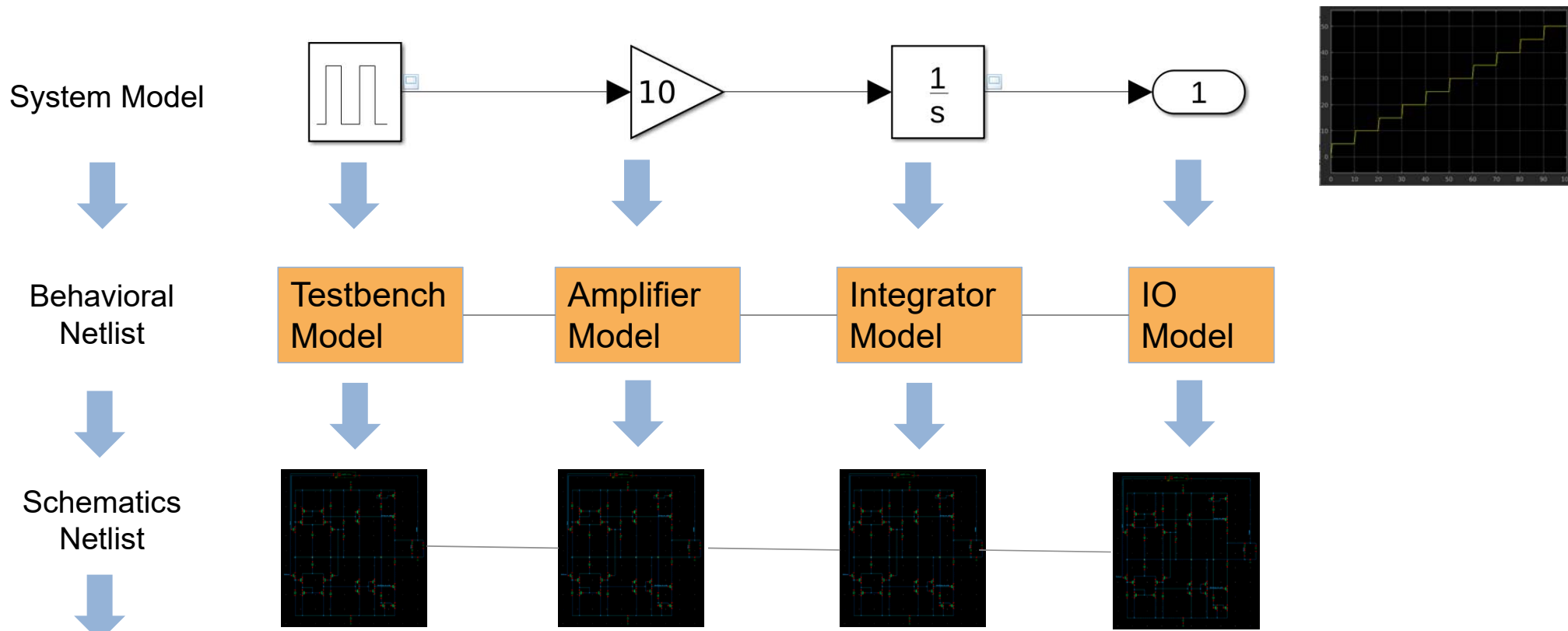
Simulation Time: Hours to Days

Other Pitfalls Of Bottoms-up Analysis

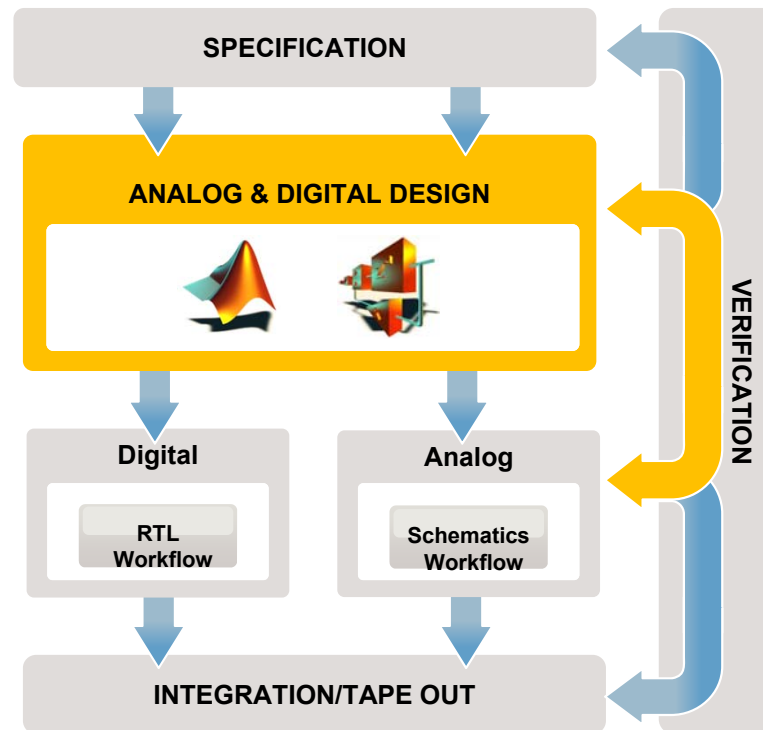


What is Top Down Modeling and Analysis

Integrating a pulse train



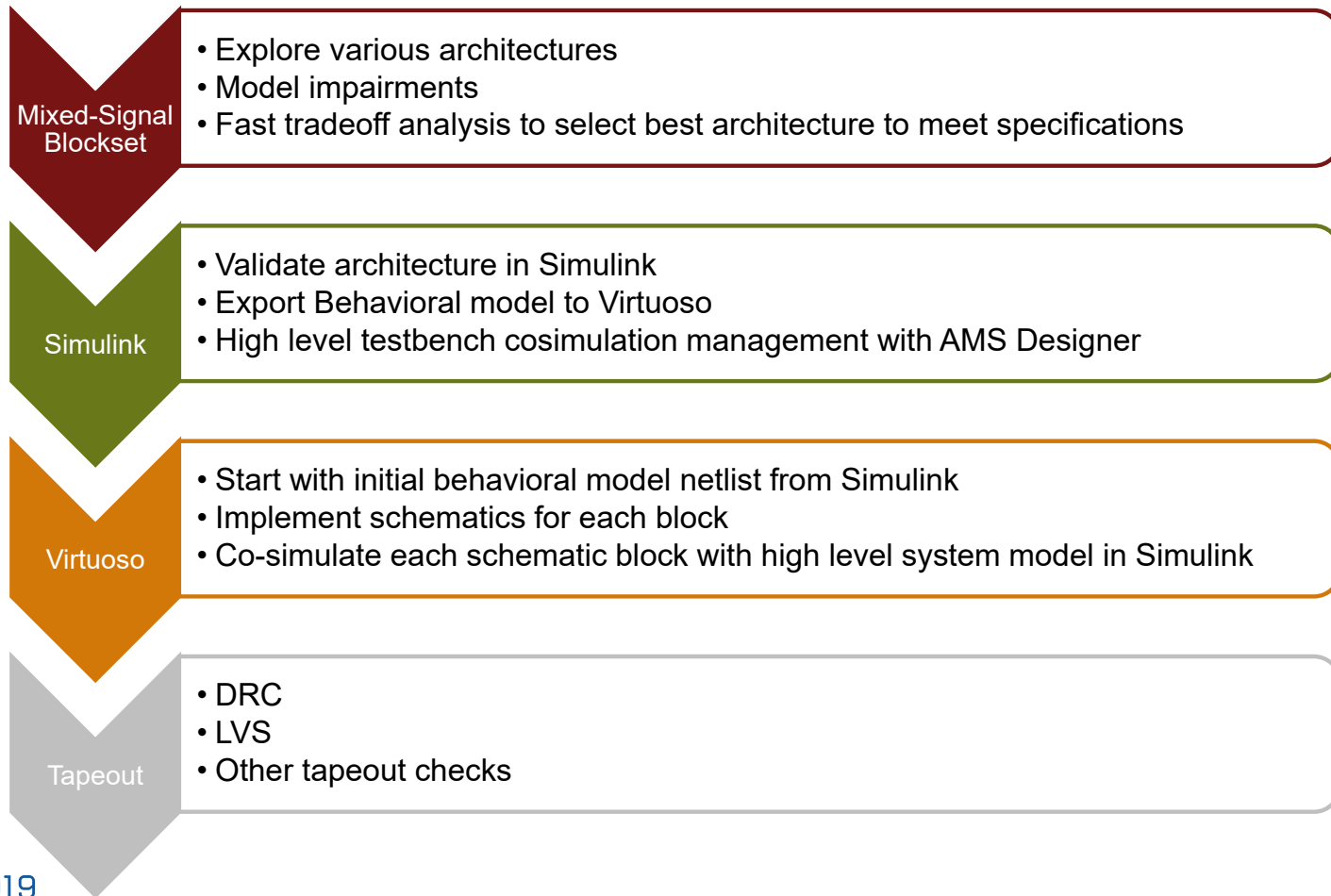
What is Top Down Analog Mixed-Signal Design



EE Times - Top-down verification guides mixed-signal designs
[Ken Kundert and Henry Chang, Partners, Designer's Guide Consulting, Los Altos, CA](#)

"In a top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as Matlab or Simulink. From the high-level simulation, requirements for the individual circuit blocks are derived."

Usage of Tools in a Top Down AMS Framework

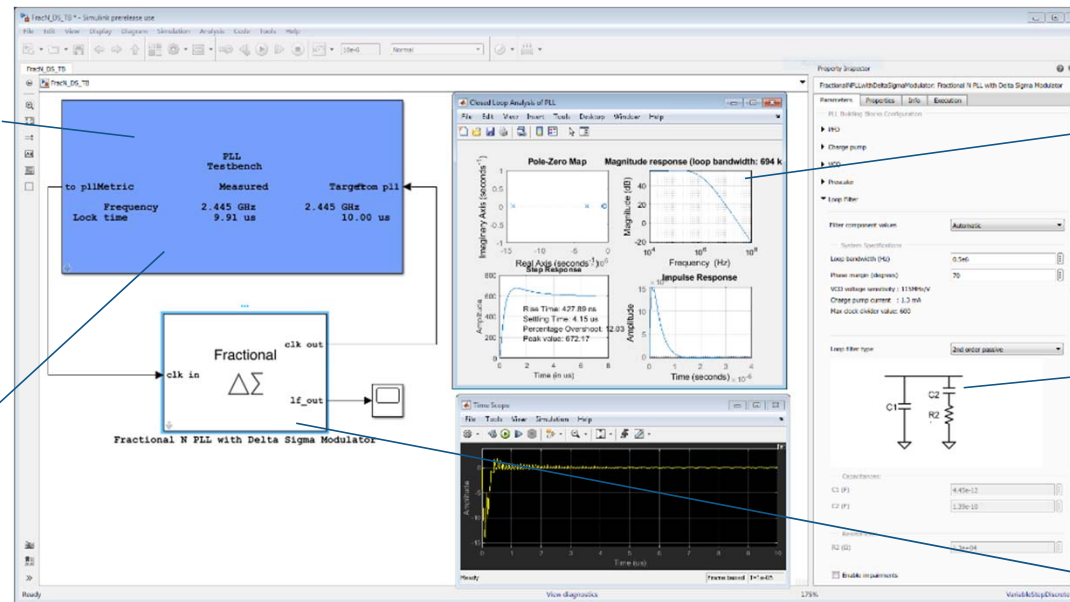
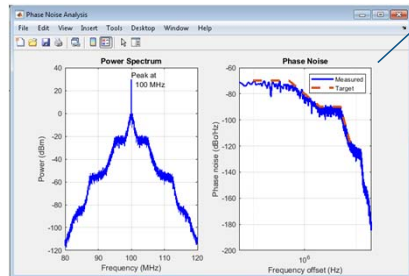


PLL Design

Architectural Selection With Mixed-Signal Blockset

Measurement testbenches

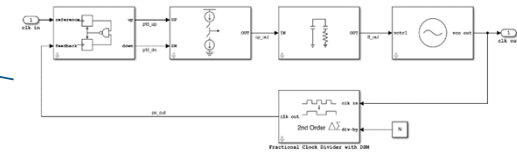
Phase noise analysis



Open and closed-loop analysis

Building blocks with impairments

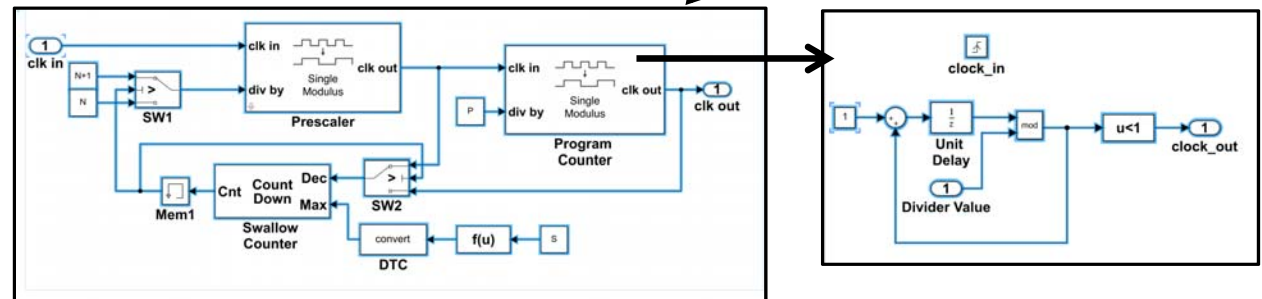
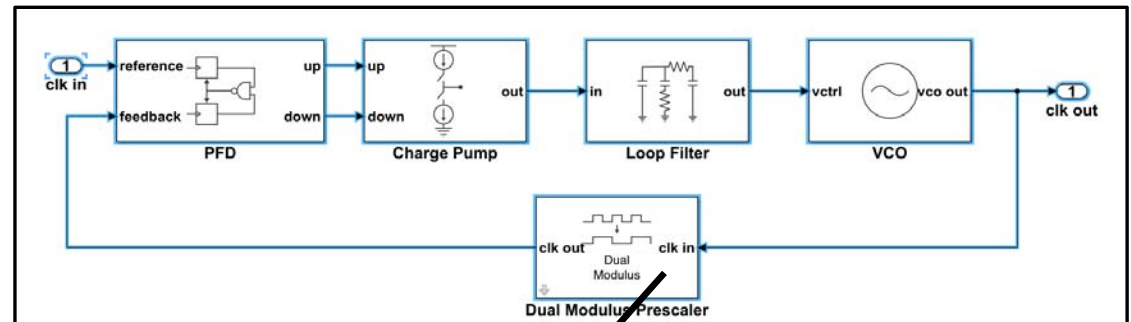
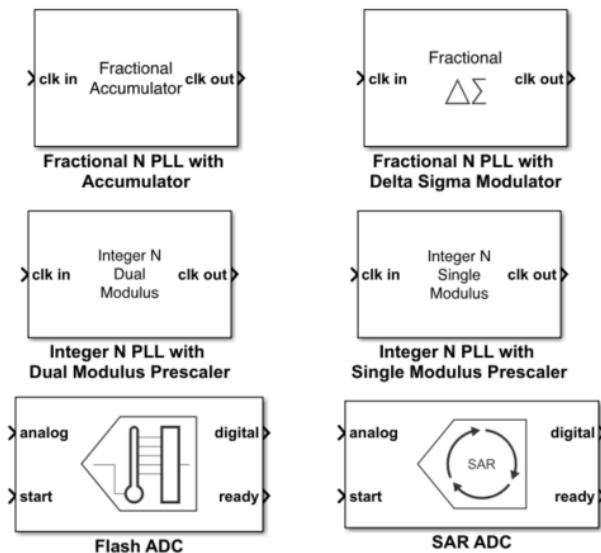
White-box architectural models



Explore Various PLL Architectural Models

Model PLL and ADCs using architectural models

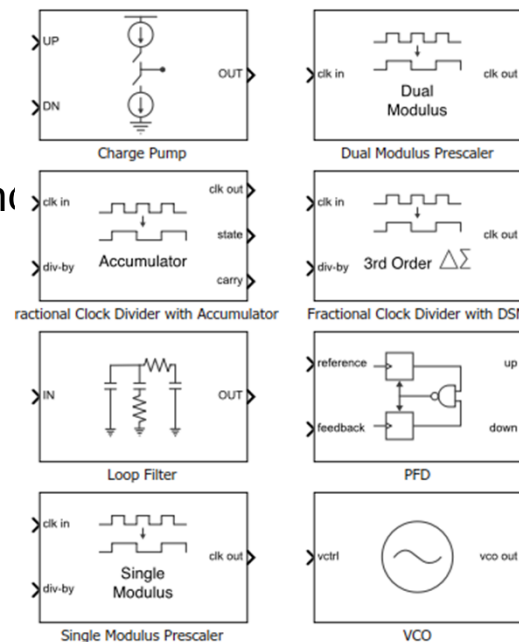
- Integer-N PLLs
- Fractional-N PLLs
- Flash, SAR ADCs



PLL Model Refinement –Impairments

- Get started in your design using building blocks including impairments

- Finite rise and fall time
- Leakage, imbalance
- Phase noise
- Aperture jitter
- PLL lock time and frequency
- PLL phase noise profile



Block Parameters: Fractional N PLL with Delta Sigma Modulator

FractionalNPLLwithDeltaSigmaModulator (mask) (link)

Frequency synthesizer with delta sigma modulator based fractional N PLL architecture.

PLL Building Blocks Configuration

PFD Charge pump VCO Prescaler Loop Filter Probe Analysis

Configuration

Output current (A)

Input threshold (V)

Impairments

☒ Enable impairments

Current Impairments

Current imbalance (A)

Leakage current (A)

Timing Impairments

Output step size calculation

☒ Default

☐ Advanced

Up

Rise/fall time (s)

Minimum Up propagation delay: 49ps

Propagation delay (s)

Down

Rise/fall time (s)

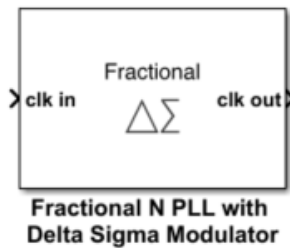
Minimum Down propagation delay: 32ps

Propagation delay (s)

OK Cancel Help Apply

Configure Each PLL Component and Run

- Model AMS behavior and impairments using your specs
- Perform open and closed-loop PLL analysis



configure

IntegerNPLLwithSingleModulusPrescaler (mask)
Frequency synthesizer with single modulus prescaler based integer N PLL architecture.

PLL Building Blocks Configuration

PFD Charge pump VCO Prescaler Loop Filter Probe Analysis

Filter component values Automatic

System Specifications

Loop bandwidth (Hz) 1e6

Phase margin (degrees) 45

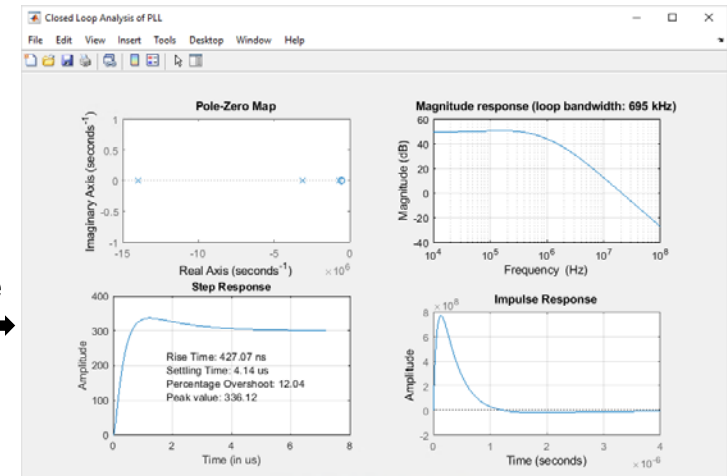
VCO voltage sensitivity : 100MHz/V

Charge pump current : 10 mA

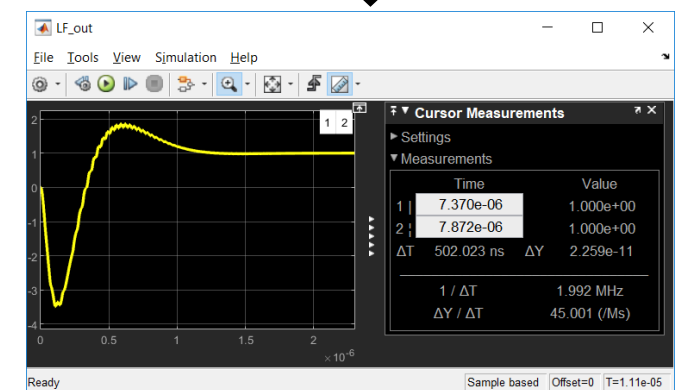
Min clock divider value : 70

Loop Filter Type 3rd order passive

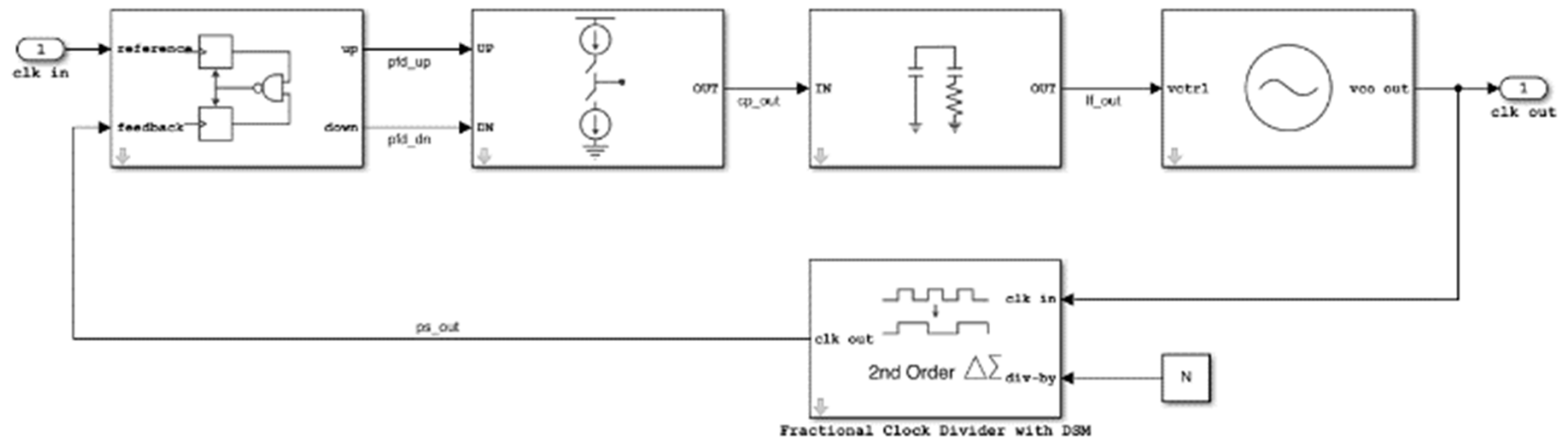
analyze



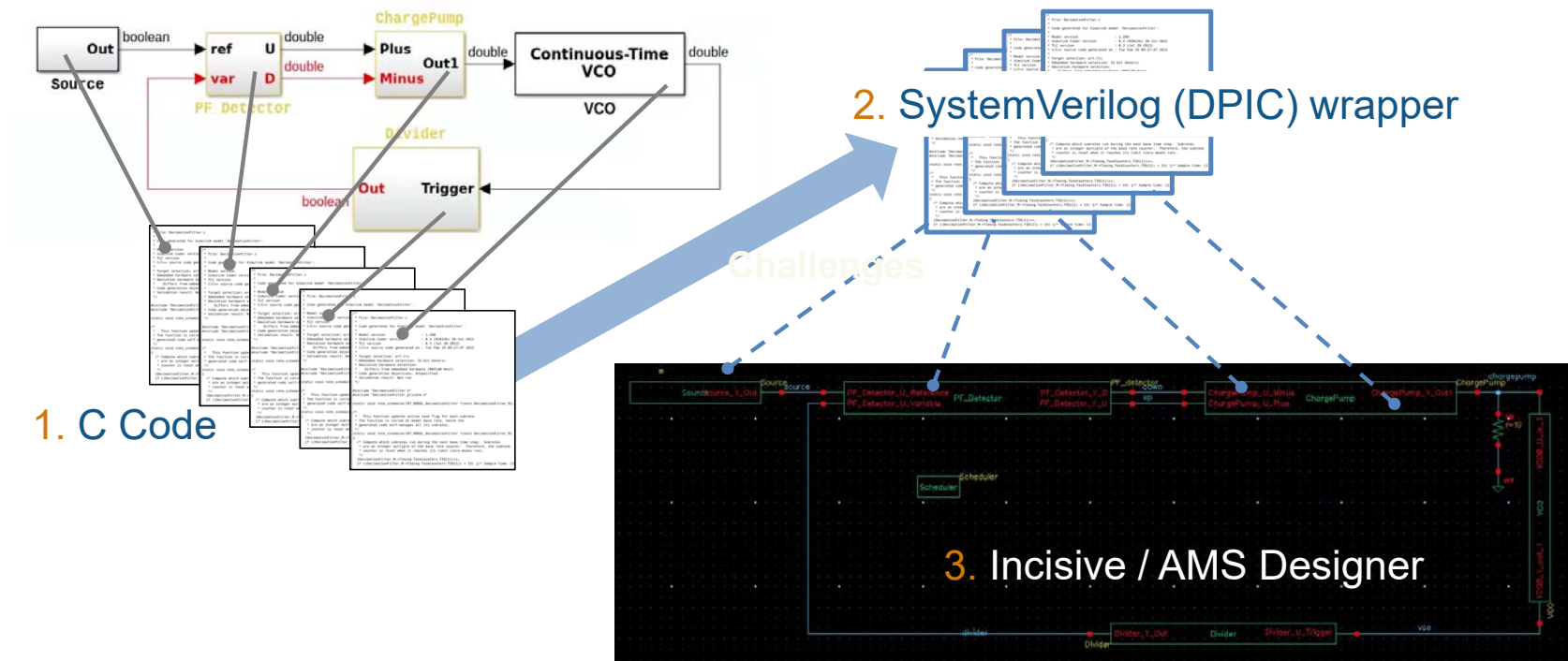
simulate



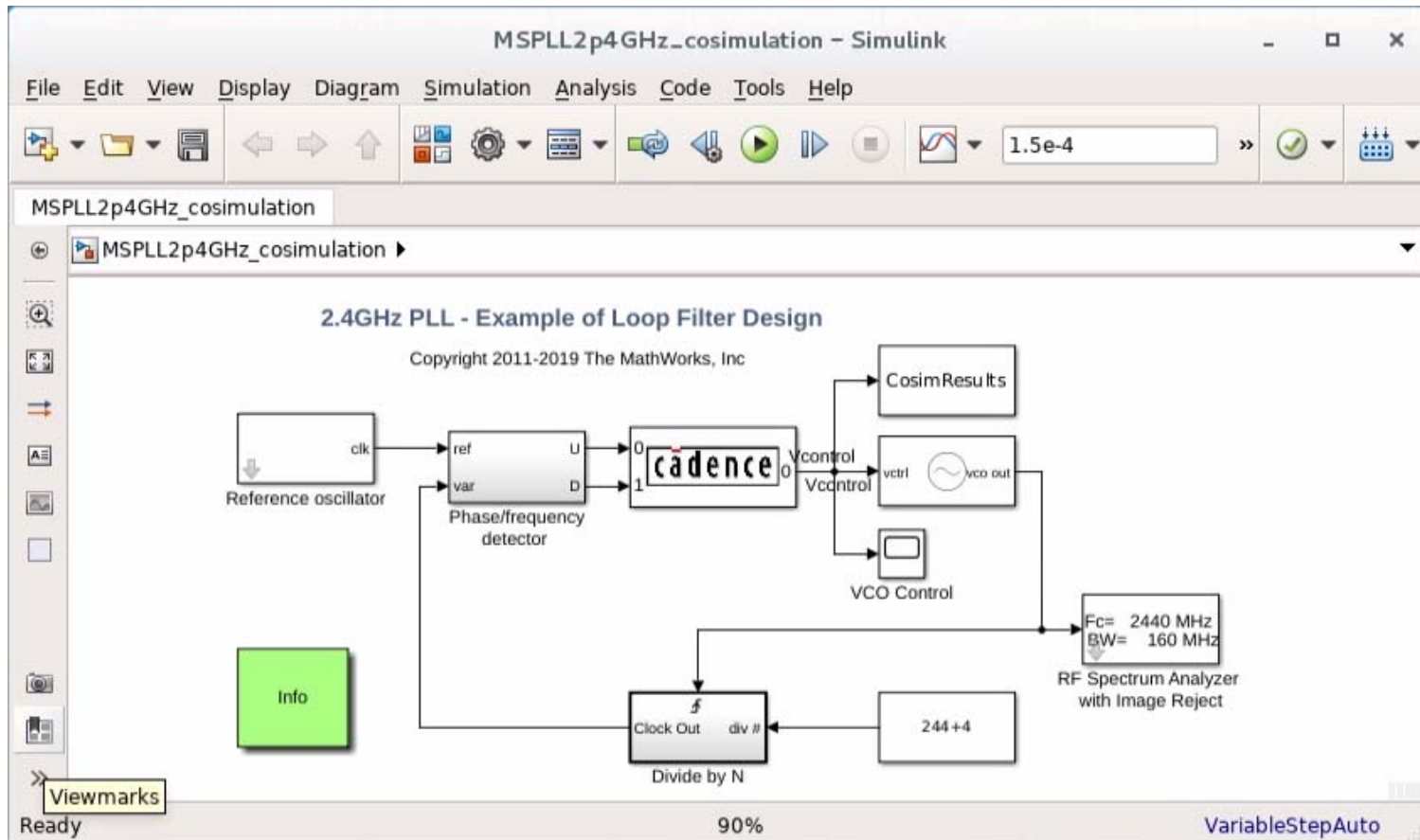
Validate Selected Architecture in Simulink

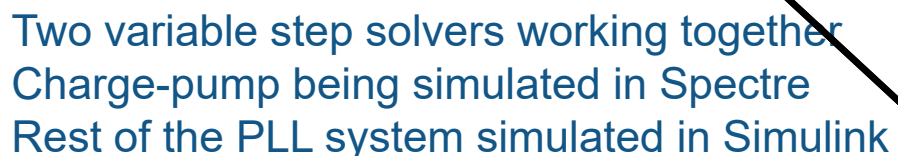


Export PLL Behavioral Model to AMS Designer

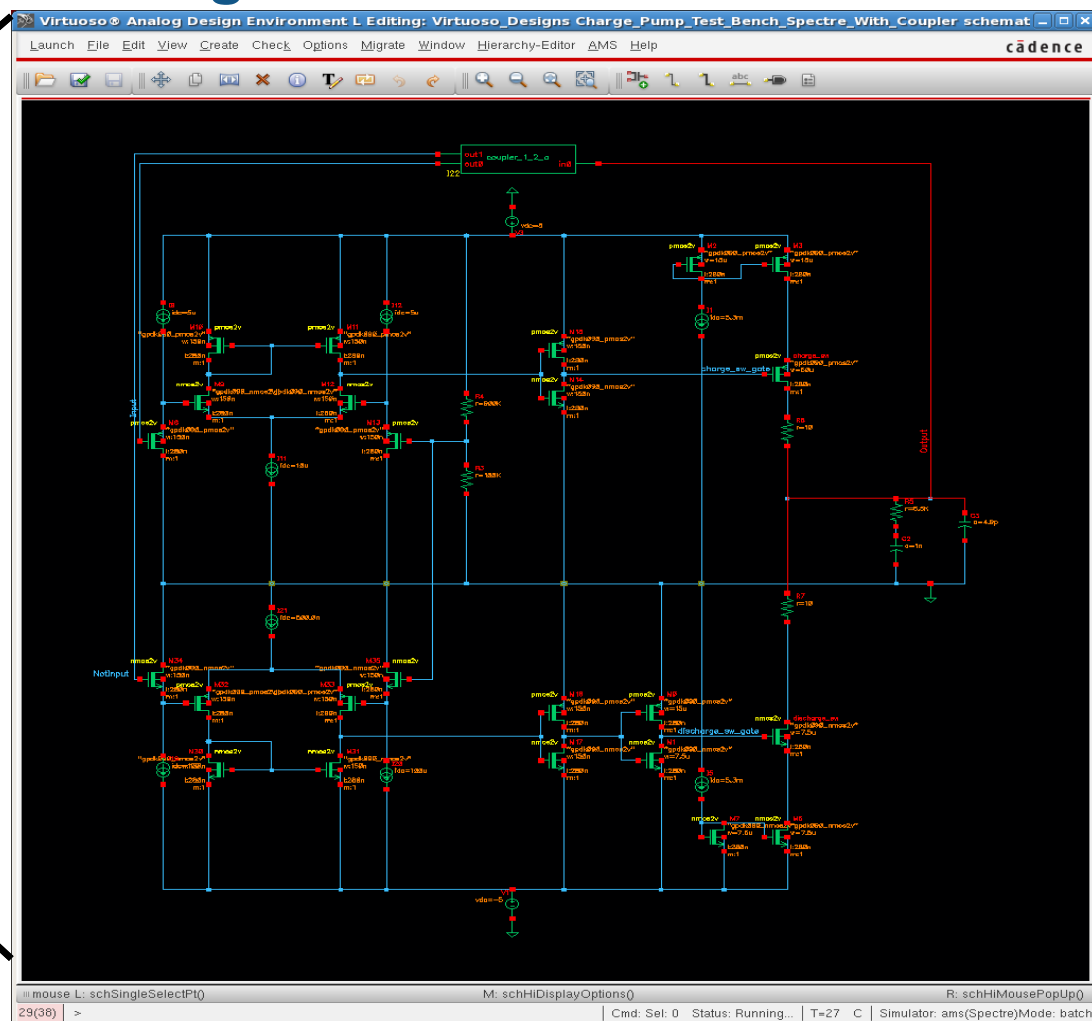


Replace PLL Charge Pump With Detailed Virtuoso Schematics

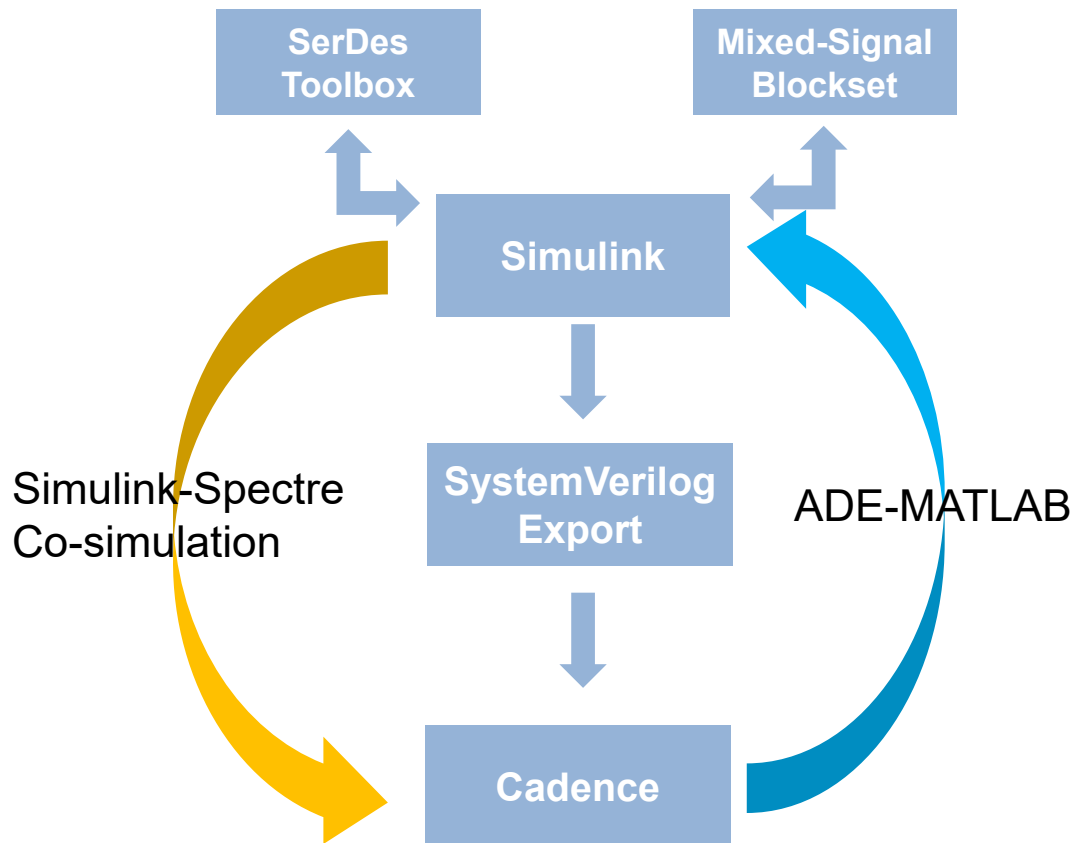




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Summarizing Top-Down AMS Tool Flow Methodology



Explore AMS Architecture in MS Blockset or SerDes Toolbox

Validate Behavioral Model in Simulink

Export Behavioral Model to Cadence

Implement AMS design in Cadence

Co-simulate Simulink with Spectre

Post process simulation data to optimize model

- PLL Tutorial
- PLL Behavioral Model with Impairments
- Voltage Controlled Oscillator including Phase Noise
- PLL 2.4GHz including Cadence Virtuoso AMS Designer Analog Cosimulation
- PLL 50x including different Measurements
- PLL with Dual Modulus Prescaler
- Fractional N PLL



Other Resources on AMS at MathWorks

- Self Paced Learning
 - [MATLAB and Simulink for Mixed-Signal Systems](#)
 - [Simulink Onramp](#)
 - [MATLAB Onramp](#)

- Available on Request
 - Hands-on Analog Mixed-Signal Workshop
 - Hands-on SerDes Workshop
 - Seminar, presentation and demo of Analog Mixed-Signal workflows